Design and Analysis of 8x8 Static RAM

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Abstract— Storage of data is required in all the high performance VLSI circuits used today. The need for the day is large amount of data to be stored and accessed as fast as possible. Approximately, after every two years, the maximum storage capacity that can be practically implemented doubles. The area efficiency of the memory array, the number of stored data bits per unit area is an important design criterion. Another important performance criterion is the memory access time. The access time determines the speed of the memory array. The area and delay are key parameters that decide the overall efficiency of an SRAM. This paper deals with designing an SRAM chip to improve the efficiency of memory array by reducing the area and observing the variations in delay for variations in process parameters. The schematics are implemented in ELECTRIC VLSI software and simulated using LTSpice.The layouts are also implemented using the same.

Index Terms - 6T, Fingering, Process parameters, SRAM, Sense Amplifier, VLSI.

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1 INTRODUCTION

WITH advancing technology, there is always an increase in demand for larger data storage capacity. This has driven the fabrication technology and memory development towards more compact design rules and towards higher data storage densities. A variety of memories are available to store and access the information stored. According to ones need one may select a read only memory which is generally used in microcontrollers or a read write memory that is generally used in microprocessors. In comparison to DRAM though SRAM requires more space, it is easily fabricated and is much faster. Dynamic RAM unlike the Static RAM needs to be refreshed after equal intervals of time. Hence for SRAMs the standby power is very low despite of high density of transistors. SRAM cells have high noise immunity due to larger noise margins, and have ability to operate at low power supplies. The most important application of SRAM is in CPU cache memories, small on-chip memories, FIFOs or other buffers. Here, we will design an 8x8 SRAM chip and analyse the area and delay of the entire chip. The chip will contain 6 transistor SRAM cells.

2 ARCHITECURE

THE name Random Access Memory is derived from the fact that the memory locations can be accessed randomly for read or write operations, irrespective of their physical locations.

The preferred architecture of the Random Access Memory is as shown in the Fig. 2.1

Each cell of the array is a 6T cell which is the core storage element. . The cell is accessed by using the row decoder and enabling the column transistors which select the appropriate row and column respectively. The precharge circuits maintain the bit and inverse bitlines high to assist the read operation. The voltage sense amplifiers are used to assist the read operation.

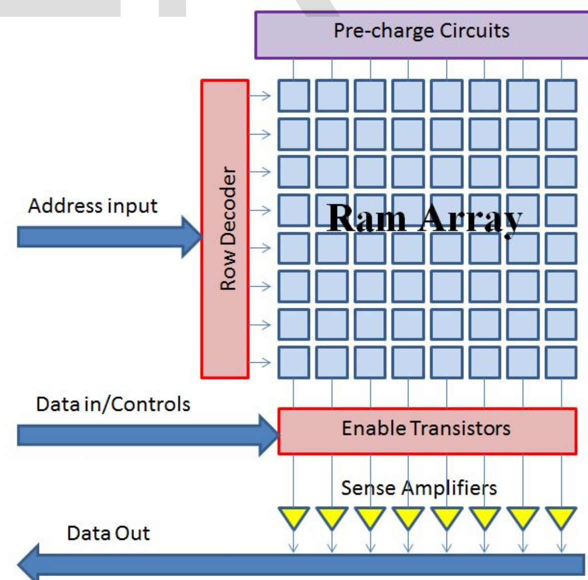

Fig. 2.1: Block Diagram

2.1 SRAM Cell

The basic Static RAM cell is the six transistor (6T) cell as shown in Fig. 2.2. The advantage of 6T cell is that static power dissipation is very less; essentially, it is limited by the PMOS transistors. It has high noise immunity [1]. In existing SRAM topologies of 8T, 9T and higher transistor count, the read static

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noise margin (SNM) is increased but size of the cell and power consumption increases relatively [2]. The 6T cell consists of two cross- coupled inverters which are formed using the transistors M1, M2, M3 and M4. The two CMOS inverters are connected such that the output of each inverter is fed to the input of the other. This feedback loop stablizes the Inverters to their respective state. It is a bistable latch. Transistors M5 and M6 are the access transistors which have their source/drain connected to the bitlines and have their gates connected to the wordline. When the cell is in standby mode the wordline is low and the access transistors are turned off.

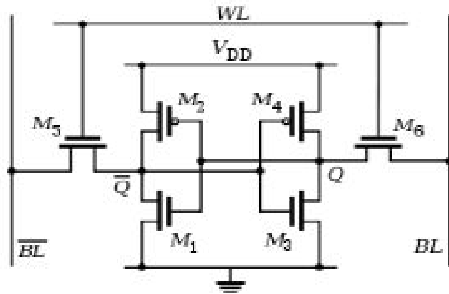

Fig. 2.2. 6T Cell

2.2 Precharge Circuit

Pre-charge plays an important role in decreasing the delay while writing bits into the memory or reading the bits from memory [3]. The bit lines are connected to a pre-charge circuit. The function of this circuit is the pull-up the two bit lines to Vdd every time the column is not selected and, in particular, before the read operations. In fact, during read operations, the two bit lines connected to the cell to be read, have to be at a certain voltage level, generally Vdd, and perfectly equalized [4]. The advantage of precharging the lines lies in the fact that only one line, either bit or bitbar is to discharge compared to the one line charged and other discharged. The pre-charge circuit used is depicted in Fig. 2.3.

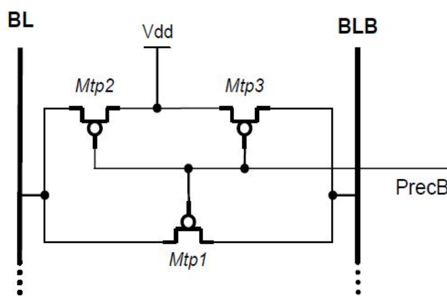

Fig. 2.3: Three Transistor Precharge Circuit

2.3 Sense Amplifier

Among all the peripherals of an SRAM memory, sense amplifier plays a major role .It is used to sense or read the data stored or written onto the selected memory bit. A sense amplifier plays the role of sensing the differential voltage generated on the bit line or bit line bar according to the data stored in the memory and accordingly convert the data stored on the bit line/bit line bar to full logic level ”1” or ”0” which can be read at the output stage. When wordline is enabled, differential begins to develop on the bit-lines which is then transferred to the sense amplifier nodes through the column select pass gate.When enough differential has developed on the sense nodes, enable is pulled high and one of the sense amplifier output is pulled low, while the other output remains high [5]. The voltage sense amplifier is as shown in Fig. 2.4.

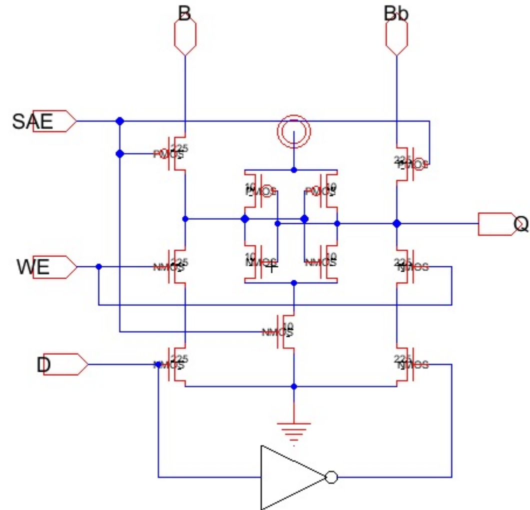

Fig. 2.4. Voltage Sense Amplifier

2.4 Row Decoder

The row decoder selects one of the 2N lines as per the address lines. The output of the decoder is fed to the wordlines in the RAM array. They select the row of the SRAM array which is to be accessed. The schematic of the row decoder used is as shown in Fig. 2.5.

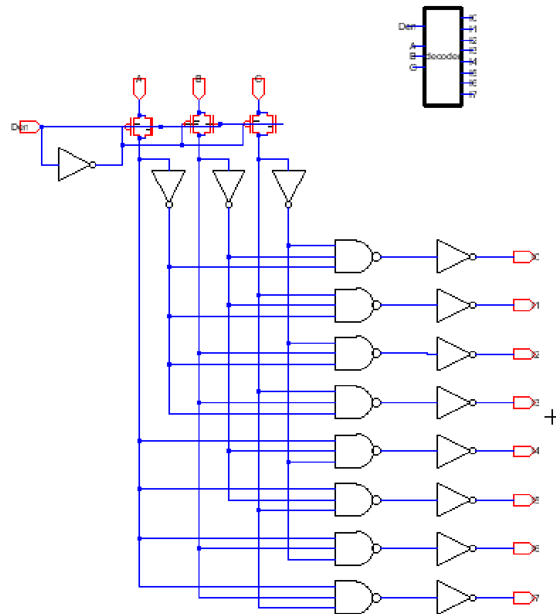

Fig. 2.5. Row Decoder

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3 Design

SIZING of individual components is the main aspect in the design of SRAM array. The sizing of each is discussed in the following sections.

3.1 6T Cell

In 6T cell for the read stability, it is necessary that the transistor M1 and M3 are larger than access transisors M5 and M6 respectively. For this the ratio of size of access transistors to the size of NMOS transistors in the CMOS inverter is given by (1). The ratio of size of PMOS transistors to size of access transistors is given by (2)

$$\frac{W_5}{W_1} = \frac{2(V_{DD} - 1.5V_{tn})V_{tn}}{(V_{DD} - 2V_{tn})^2} \quad (1)$$

$$\frac{W_5}{W_2} \geq \frac{\mu_p (V_{DD} + V_{tp})^2}{\mu_n (2(V_{DD} - 1.5V_{tn}))V_{tn}} \quad (2)$$

Vtn – NMOS threshold voltage
Vtp – PMOS threshold voltage
μ_p - Mobility of holes
μ_n - Mobility of electrons
V_{DD} -Supply voltage
W_x - Width of transistor x

The 6T cell designed has layout as shown in Fig. 3.1

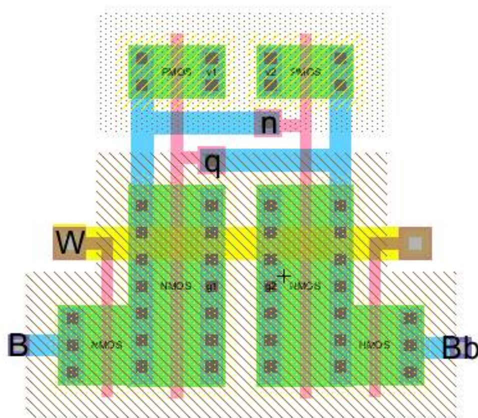

Fig. 3.1. 6T Layout

3.2 Sense Amplifier

Once the schematic is made the aspect ratio (W/L ratio) of the driver, access transistors and load transistors need to be set. The main criteria to be considered while choosing the ratio are:

1) The data of read operation should not be destructive.
2) Static noise margin should be in the acceptable range.

Since the size of the access transistors were large compared to the others, while implementing the layout the technique of fingering was used. Fingering is a technique of replacing a single transistor with large width with multiple transistors of smaller width. The advantages of fingering are: [6]

1) With even number of transistors the active capacitance reduces.
2) It helps to optimize the resistance of gate poly along the width of the transistor.

Fingering is as shown in Fig. 3.2.

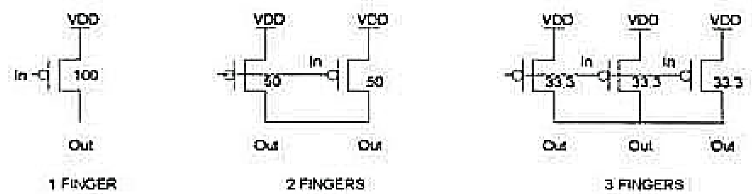

Fig. 3.2: Fingering

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The sense amplifier so designed has layout as shown in Fig. 3.3.

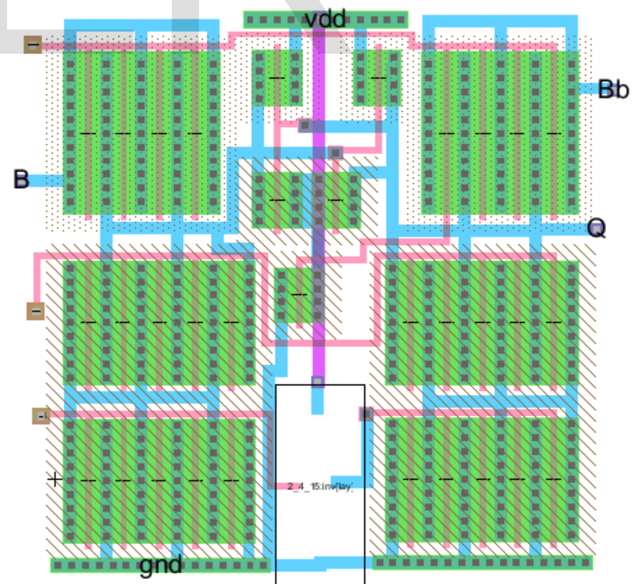

Fig. 3.3. Sense Amplifier Layout

3.3 Row Decoder

The row decoder used is 3x8. It is designed using 3 input NAND gates. The transmission gate is used as an enable for the decoder allowing the address to be passed. The sizing of

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row decoder is done by keeping the minimum sizes for the NAND and inverter layouts. The layout of the decoder designed is as shown in Fig. 3.4.

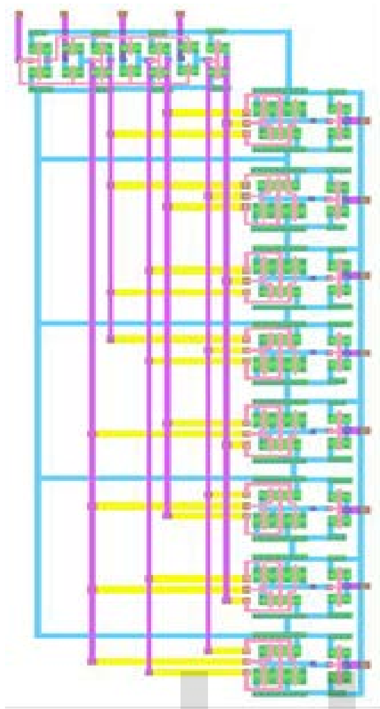

Fig. 3.4: Layout of Row Decoder

3.4 Complete SRAM chip

The layout of the 8x8 SRAM chip with the pad frame is as shown in Fig. 3.5.

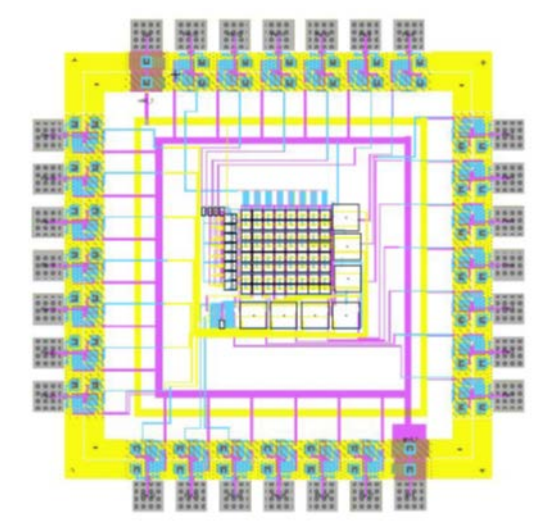

Fig. 3.5. Layout of 8 x 8 SRAM chip

4 Results and Discussions

The 8x8 SRAM is tested for variations in process parameters and the results are as shown in table 1.

FF-fast n, fast p FS-fast n, slow p
SF- slow n, slow p SS - Slow n, Slow p.
Tox – Thickness of oxide layer

During write operation, the maximum change observed is 49.37% increase and during read operation the maximum change observed is 56.79% decrease for variations in process parameters. Static Random Access Memory is designed and analysis is performed to get the desired results. The effect of variations in process parameters are observed to be within desirable range. For the SRAM chip designed, the specifications are as follows:

No of pins = 28
Capacity = 8x8 bits = 64bits
Area = 1.468 um2
Read delay = 3.5 ns
Write Delay = 4.5 ns

TABLE 1
Variations In Delay With Respect To Process Parameters For A Write Operation of 1 in 0TH Row

Write 1 in 0th row	FF	FS	SF	SS
Vdd	2.736	3.466	2.655	3.281
Vdd +10%	2.476	2.880	2.414	2.780
Vdd-10%	3.138	---	2.989	4.616
Tox +10%	2.693	3.258	2.617	3.108
Tox -10%	2.812	4.052	2.720	3.682
Tox+10%&Vdd+10%	2.445	2.789	2.383	2.705
Tox+10%&Vdd -10%	3.090	4.399	2.948	3.770
Tox-10%&Vdd +10%	2.530	3.035	2.468	2.924
Tox-10%& Vdd -10%	3.233	---	3.071	---

TABLE 2
Variations In Delay With Respect To Process Parameters For A Write Operation of 0 in 7TH Row

Write 0 in 7th row	FF	FS	SF	SS
Vdd	2.118	2.375	2.022	2.248
Vdd +10%	2.089	2.448	2.001	2.308
Vdd-10%	2.127	---	2.029	---
Tox +10%	2.115	2.357	2.020	2.245
Tox -10%	2.120	2.414	2.031	2.277

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Tox+10% & Vdd +10%	2.081	2.369	1.996	2.258
Tox+10% & Vdd -10%	2.131	---	2.035	---
Tox-10% & Vdd +10%	2.111	2.590	2.025	2.398
Tox-10% & Vdd -10%	2.139	---	2.031	---

TABLE 3

VARIATIONS IN DELAY WITH RESPECT TO PROCESS PARAMETERS FOR A READ OPERATION OF 1 IN 0TH ROW

Read 1 from 0th row	FF	FS	SF	SS
Vdd	2.161	2.824	2.178	2.788
Vdd +10%	2.006	2.067	1.371	2.075
Vdd-10%	3.271	---	3.252	1.247
Tox +10%	2.162	2.844	2.178	2.806
Tox -10%	2.160	2.814	2.178	2.776
Tox+10% & Vdd +10%	2.007	2.067	2.014	2.075
Tox+10% & Vdd -10%	3.293	1.151	3.273	1.280
Tox-10% & Vdd +10%	2.006	2.068	2.014	2.076
Tox-10% & Vdd -10%	3.257	---	3.236	---

TABLE 4

VARIATIONS IN DELAY WITH RESPECT TO PROCESS PARAMETERS FOR A READ OPERATION OF 0 IN 7TH ROW

Read 0 from 7th row	FF	FS	SF	SS
Vdd	2.657	2.709	2.571	2.627
Vdd +10%	2.575	2.690	2.496	2.611
Vdd-10%	2.713	---	---	---
Tox +10%	2.701	2.764	2.616	2.684
Tox -10%	2.619	2.661	2.532	2.577
Tox+10% & Vdd +10%	2.608	2.723	2.527	2.646
Tox+10% & Vdd -10%	2.758	---	---	---
Tox-10% & Vdd +10%	2.554	2.662	2.472	2.580
Tox-10% & Vdd -10%	2.670	---	2.628	---

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5 CONCLUSION

This paper analyses an 8x8 SRAM chip for area reduction and for variations in process parameters. The SRAM consists of 6T cell as the storage element, row decoder as the addressing element, and sense amplifier along with enable transistors for read and write operations. The layouts of the individual components are designed and put together to get the complete layout of 8x8 SRAM chip. The chip consists of 28 pins and has an area of 1.468 um^2. The design was tested for variations in process parameters.

The SRAM is a vast topic of study and further improvements in power and area are possible. Also the number of pins can be reduced by including a controller in the chip for I/O interface allowing the chip to be easily connected to other processors and systems.

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